CE4940 WINTER 2016-2017 HOMEWORK HW7

Design a 3-bit prime number recognizer. The output PRIME = 1 if and only if input number ABC is a prime number where A is the most-significant numerical bit. **Use** the mathematical definition of PRIME as a number >1.

Use the following table of values to complete RTL, CMOS, and Pseudo-NMOS implementations.

NMOS	VTO=0.4V	KP = 80µA/V^2	L = 1.2µm
PMOS	|VTO| = 0.4V	KP = 32µA/V^2	L = 1.2 µm
VDD	5V		
VOL for RTL and Pseudo	0.2V		
Rsheet for RTL	25Ω		

Complete SPICE simulation of each solution: RTL, CMOS, and Pseudo. **Include** DC stepped voltage simulation for the reference inverter. **Include** transient simulation for the complex logic circuit that shows the entire 8-item number as well as supplied power.

Include an area, transistor count, and power comparison table for all three solutions. **Assume** the interconnect lengths are 0 and all components are sitting right next to each other. Remember that the equation for resistance of material can be found by: $R = R_{sheet} * \left(\frac{W}{L}\right) \Omega$.

You may submit either paper solution or PDF to the instructor. Your submission packet is due by Friday at 5 p.m. in Week 8.